# SEMICONDUCTOR DEVICE WITH SPEED BINNING TEST CIRCUIT AND TEST METHOD THEREOF

This application claims the priority of Korean Patent Application No. 2003-839, filed on January 7, 2003 in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

## BACKGROUND OF THE INVENTION

### Field of the Invention

[0001]    The present invention relates to a semiconductor device with a speed binning test circuit and a test method thereof.

### Description of the Related Art

[0002]    In general, semiconductor memory devices such as a Dynamic Random Access Memory (DRAM) and an Application-Specific Integrated Circuit (ASIC) are manufactured by a series of processes.   These processes may include a design process, a manufacture process, a chip test process, and a packaging process, before the semiconductor memory devices enter the marketplace.   One type of chip test process is referring to as a speed binning test. A speed binning test is one of a series of processes performed after the manufacture process. In high-performance semiconductor memory devices such as those described above, a significant effect of temperature variation during testing is to affect the assessed maximum speed of the device in normal use, known as "speed binning". In a speed binning test, operation speeds of chips may be measured at a wafer-level, and poor-quality chips or wafers may be sorted out based on the result of measurement.

[0003]    The operation speeds of semiconductor integrated circuits such as central processing units (CPUs), which are manufactured through an ultra-fine process, rely largely on process variations.   Thus, there is a need for monitoring on-chip variations at a wafer level using the speed-binning test, and then predicting the operation features of chips, prior to placing the chips in the marketplace. Accordingly, packaging costs may be reduced. Typically, product costs for packaging a device such as a high-performance CPU is expensive, and the practical utility of working dies is determined primarily by the dies' functional working at a desired speed, rather than the dies' functional

working. Therefore, it is more desirable to perform the speed-binning test at the wafer level to sort out poor-quality wafers.

[0004] In a conventional speed binning test circuit, a Boundary Scan Register (BSR) installed within the chip may be used to measure turn-around time by using an inverter chain installed around the chip. The turn-around time indicates a delay time duration until an input signal is output. Turn-around time is used for estimating the operation speed of the chip after the packaging process. That is, the range of the chip operation speed may be estimated using tracking plots that are measured based on a correlation between the turn-around time from the inverter chain, and the chip operation speed. The speed-binning test described above is disclosed in US Patent Application No. US20020129310A1.

[0005] A conventional speed binning test method of measuring turn-around time is based on the fact that the operation speed of chip (using the inverter chain and DC characteristics evaluated through a Test Element Group (TEG), for example) depend largely on process variations.

[0006] However, as process conditions become more minute and on-chip variations become more serious, it is difficult to accurately predict the operation speed of chip by only using the conventional inverter chain to measure the turn-around time after the packaging process. In other words, the influences of on-chip variations upon circuits at every possible location, e.g., upper, lower, left and right portions, over the chip are represented as a data value, which may be referred to as a 'total delay value', in the inverter chain. It is impossible to accurately predict the operation speed based only on the total delay time. For example, it is difficult to determine whether (i) circuits at the every possible location over the chip are affected uniformly by the on-chip variations, or (ii) only a circuit at a particular location is largely affected by the on-chip variations. Thus, it may be difficult to explain why the operation speed of a core circuit becomes slower when the turn-around time for the latter case (ii) equals turn-around time for the former case (i).

[0007] Also, in the conventional speed binning test method, influence of on-chip variations is evaluated by manually measuring operation speeds at a number of different locations in the inverter chain (which is installed around the core circuit), using test equipment. The results of these measurements

are then stored in a database. However, considerable time is spent on manual evaluation of the operation speed, thus making it difficult to measure the operation speeds of all of chips on a wafer. Accordingly, in the above test method only a few wafers of a lot are selected, and the evaluation is performed on only a few chips of the selected wafers. A distribution of measurement results become wide, as process conditions become even more minute. Thus, these measurement results are not accurate enough to represent the performance of the all chips on a wafer.

## SUMMARY OF THE INVENTION

[0008] Exemplary embodiments of the present invention are directed to a speed binning test circuit that may include a plurality of circuit groups arranged along a boundary of a chip of a semiconductor device. Each circuit group may include a different number of unit delay circuits that may form a chain structure on the chip. The speed binning test circuit may also include a plurality of pads. Each pad may be arranged on the chip between a pair of circuit groups so that at least one output terminal of a unit delay circuit of one of the plurality of circuit groups is connected to one of the pads. The speed binning test device may perform a speed binning test method in which a signal through the circuit groups is delayed, and on-chip-variations are monitored to determine a total signal delay time through the chain structure.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Exemplary embodiments of the present invention will become more fully understood from the detailed description herein below and the accompanying drawings, wherein like elements are represented by like reference numerals, which are by way of illustration only and thus do not limit the exemplary embodiments of the present invention and wherein:

[0010] FIG. 1 is a block diagram illustrating a structure of a semiconductor device with a speed binning test circuit according to an exemplary embodiment of the present invention;

[0011] FIG. 2 is a block diagram illustrating speed correlation circuits shown in FIG. 1.

**[0012]** FIG. 3 illustrates an oscillation waveform used when measuring the operation speeds of the speed correlation circuits shown in FIG. 2.

## DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

**[0013]** Hereinafter, exemplary embodiments of the present invention will be described in detail with reference the accompanying drawings. The same reference numerals represent the same elements throughout the drawings.

**[0014]** FIG. 1 is a block diagram illustrating a structure of a semiconductor device with a speed binning test circuit that performs a speed-binning test, according to an exemplary embodiment of the present invention. Referring to FIG. 1, the semiconductor device, which in FIG. 1 is embodied as a chip, for example, may include a plurality of signal input/output (I/O) pins (not shown), which are the same as those installed in a general semiconductor device, for example. Signals may be input to the signal I/O pins from a core circuit 110, and/or signals may be output from the signal I/O pins to the core circuit 110. The core circuit 110 performs given functions using its logic circuit and receives/outputs signals from/to the plurality of signal I/O pins.

**[0015]** A speed binning test circuit is arranged around core circuit 110. The speed binning test circuit includes a plurality of (known) unit delay circuits (hereafter 'unit delay circuits' for clarity) and a plurality of pads. As shown in FIG. 1, the unit delay circuits may be categorized into four groups (first through fourth groups). These four groups may be represented as first speed correlation circuit 120, second speed correlation circuit 130, third speed correlation circuit 140 and fourth speed correlation circuit 140. The first through fourth groups may be arranged along the boundary of the core circuit 110 in a chain structure, for example. The total number of unit delay circuits within each of the respective first through fourth groups may be different. For example, the ratio of the numbers of unit delay circuits in each of the four groups may be expressed as follows in equation (1):

$$A:B:C:D = a:b:c:d \qquad \ldots (1).$$

In equation (1), $A$ denotes a number obtained by subtracting 1 from the number of unit delay circuits of the first group; $B$ denotes the number of unit

delay circuits of the second group; C denotes the number of the unit delay circuits of the third group; D denotes the number of the unit delay circuits of the fourth group. The parameters a, b, c, and d may be any different numbered coefficients.

[0016] In the speed binning test circuit, the first speed correlation circuit 120 may include a plurality of serially-connected unit delay circuits that constitute the first group. The first speed correlation circuit 120 delays a final delay signal received from fourth speed correlation circuit 150, via pad 160, and outputs the delayed final delay signal as a first delay signal. The second speed correlation circuit 130 may include a plurality of serially-connected unit delay circuits that constitute the second group. The second speed correlation circuit 130 delays the first delay signal and outputs the delayed first delay signal as a second delay signal. The third speed correlation circuit 140 includes a plurality of serially-connected unit delay circuits that constitute the third group. The third speed correlation circuit 140 delays the second delay signal and outputs the delayed second delay signal as a third delay signal. The fourth speed correlation circuit 150 includes a plurality of serially-connected unit delay circuits that constitute the fourth group. The fourth speed correlation circuit 150 delays the third delay signal and outputs the delayed first signal as the final delay signal. Each of a plurality of pads 160 is connected to at least one output terminal of the unit delay circuit of the first through fourth groups, respectively.

[0017] The first through third delay signals and the final delay signal have the same oscillation waveforms after a given time. The given time is a total signal delay time Dt delayed in the chain formed by the unit delay circuits of the first through fourth groups.

[0018] FIG. 2 is an exemplary block diagram of the first through fourth speed correlation circuits 120 through 150 shown in FIG. 1. Referring to FIG. 2, the first through fourth speed correlation circuits 120 through 150 are installed in a chain structure around the boundary of core circuit 110 and include given (known or determined in advance) unit delay circuits, i.e., inverter circuits. However, the unit delay circuits according to the exemplary embodiments of the present invention are not limited to inverter circuits. The unit delay circuits may embodied as any circuit capable of inverting input

signals and outputting an inverted, and/or as buffers capable of outputting signals having the same phases as signals input thereto. However, if the unit delay circuits are buffers, at least one of the unit delay circuits should be an inverter circuit so that the chain structure can operate as a ring oscillator.

[0019] The speed correlation circuits 120 through 150 form four groups of unit delay circuits, i.e., inverter circuits. The total numbers of inverter circuits in a given group may be different then numbers in another group, the ratio of which as shown in equation (1).

[0020] Referring to FIG. 2, the number of inverter circuits of the first group are represented as (N+1); those of the second group as 2N, those of the third group as 3N, and those of the fourth group as 5N. The number of inverter circuits in first group is set at N+1 so that the total number of inverter circuits in all four groups are an odd number. By having an odd number of total inverter circuits, the chain structure may act as a ring oscillator. The ratio of numbers of inverter circuits of the first through fourth groups may be approximately 1:2:3:5 when N may be several tens or several hundreds of inverter circuits. The parameters a, b, c, and d of equation (1) may be any numbers, so long as the for numbers are different form each other. It may be easier to evaluate the influence of on-chip variations if a, b, c, and d are set as different prime numbers.

[0021] Assuming that a signal delay time delayed in the first speed correlation circuit 120 is D, signal delay times in the second through fourth speed correlation circuits 130 through 130 are approximately 2D, 3D, and 5D, respectively. A 'derating factor' is a value that indicates the degree of influence of on-chip variations to the operation speed of a circuit. If the derating factors of the first through fourth speed correlation circuits 120 through 150 are the same, a total signal delay time 'Dt' in the first through fourth speed correlation circuits 120 through 150 may be computed as follows by equation (2):

$$Dt \fallingdotseq D + 2D + 3D + 5D \quad \ldots (2).$$

[0022] If the degrees, i.e., the derating factors, of the influence of on-chip variations upon the operation speeds of the first through fourth speed correlation circuits 120 through 150 are different from one another, the total signal delay time Dt may be calculated as follows using equations (3) or (4):

$$Dt \doteqdot 0.9D + 1.1^*(2D) + 3D + 5D \quad \dots (3)$$

$$Dt \doteqdot 0.9D + 1.1^*(2D) + 1.4^*(3D) + 0.6^*(5D) \quad \dots (4)$$

However, the computation of total signal delay time Dt is not limited to calculations performed by equations (3) and (4); rather, the computation of Dt varies, depending on on-chip variations.

[0023] Referring to equations (2) through (4), the total signal delay time Dt related to the same derating factors is not the same as the total signal delay time Dt related to different derating factors. If a, b, c, and d of equation (1) are different prime numbers, it is easier to evaluate the influence of the on-chip variations. In other words, since a, b, c, and d may only be evenly divided by 1 or by itself, it may be easier to determine the correlation among the total signal delay time Dt and the derating factors of the speed correlation circuits 120 through 150.

[0024] The conventional speed binning test method evaluates an operation speed merely by measuring a turn-around time using an inverter chain formed with inverter chain groups having the same number of inverter circuits in each group. For this reason, it is difficult to determine, using the conventional speed binning test method, whether circuits at the every possible location over the chip are uniformly affected by on-chip variations, or if only a circuit at a particular location is affected by the on-chip variation. This is because signal delay times Dt are the same for the above two cases.

[0025] In accordance with the exemplary embodiments of the present invention, however, the numbers of the inverter circuits in each of the first through fourth groups are different. Therefore, the extent of the influence of on-chip variations (i.e., the derating factors) on circuits at various locations in

the chip may be more easily and individually determined, since total signal delay time Dt is measured only once. Further, the exemplary embodiments of the present invention may make it easier to monitor circuits at several locations on a timing-critical chip, so as to determine those circuits on the chip that may be substantially affected by on-chip variations.

[0026] FIG. 3 illustrates an oscillation waveform used when measuring the operation speeds of the speed correlation circuits shown in FIG. 2. The oscillation waveform shown in FIG. 3 may be observed by probing signals output from the pads 160 using probe cards and an oscilloscope. Each pad 160 is connected to at least one output terminal of the unit delay circuits of the four groups, respectively.

[0027] The first through fourth speed correlation circuits 120 through 150 may be connected to one another in a chain structure so as to act as a ring oscillator, for example. Thus, the first through third delay signals (and the final delay signal), have the same oscillation waveforms after a given time. The given time is a total signal delay time delayed in the chain structure formed from the unit delay circuits of the four groups. The total signal delay time Dt in the first through fourth speed correlation circuits 120 through 150 may be computed using the frequency of the signal waveform, shown in FIG. 3, which is obtained by probing signals output from pads 160. If the frequency of the signal waveform is f, the total signal delay time Dt can be expressed as by equation (5), for example:

$$Dt = 1/(2f) \quad \dots (5)$$

[0028] As described above, in a semiconductor device according to an exemplary embodiment of the present invention, a speed binning test circuit may be provided for performing a speed binning test procedure. Generally, the test method includes delaying a signal through each successively connected circuit groups ('group'), where each group includes a different number of unit delay circuits that form of a chain structure, and monitoring on-chip-variations to determine total signal delay time delayed in the chain structure. Each group may include a given different number of unit delay circuits, as discussed above. On-chip variations may be monitored by

observing an oscillation waveform of signals output from each of the pads, where each pad is connected to at least one output terminal of the unit delay circuits of the four groups, respectively.

[0029]    As described above, an inverter chain in accordance with the exemplary embodiments of the present invention may be constructed differently from a conventional inverter chain.    Thus, one-time measurement of total signal delay time Dt allows measurement of the degrees, i.e., derating factors, of the influence of on-chip variations upon the operation speeds of circuits installed at a variety of locations, e.g., upper, lower, left, and right portions, on the chip.    Also, the speed binning circuit and test method in accordance with the exemplary embodiments of the present invention may facilitate monitoring of on-chip variations in operation speeds of circuits at a plurality of locations on a timing-critical chip.    Accordingly, this may improve the accuracy in sorting out circuits on the chip that may be substantially adversely affected by the on-chip variations, so as to minimize error in predicting operation speed of a chip.    This may help to reduce product costs, and provide a more efficient way to evaluate the influence of the on-chip variations in chips of entire wafers in a lot.

[0030]    The exemplary embodiments of the present invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as departure from the spirit and scope of the exemplary embodiments of the present invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.